****

**EXAMINATION PAPER**

**FACULTY : COMPUTER SCIENCE AND MULTIMEDIA**

**COURSE : BACHELOR OF INFORMATION TECHNOLOGY (Hons.)**

**YEAR/ SEMESTER : FIRST YEAR / SEMESTER TWO**

**MODULE TITLE : DIGITAL LOGIC**

**CODE : BIT 126**

**DATE : SEPTEMBER 20 – 2018, THURSDAY**

**TIME ALLOWED : 3 HOURS**

**START : 1:00 PM FINISH : 4:00 PM**

**Instruction to candidates**

1. This question paper has THREE (3) Sections.
2. Answer **ALL** questions in Section A, MCQ.
3. Answer **5** questions in Section B, MSAQ.
4. Answer **2** questions in Section C, MEQ.
5. No scripts or answer sheets are to be taken out of the Examination Hall.
6. For Section A, answer in the OMR form provided.

***Do not open this question paper until instructed***

**SECTION A**

**Multiple Choice Questions (30\*1=30)**

1. **3x8 decoder will have:**
2. 4 outputs
3. 5 outputs
4. 6 outputs
5. 8 outputs

1. **What is the function of an enable input on a multiplexer chip?**
2. To apply Vcc
3. To connect ground
4. To active the entire chip
5. To active one half of the chip
6. **How many types of parity bits are found?**
7. 2
8. 3
9. 4
10. 1
11. **Decimal digits are displayed on:**
12. Input
13. Output
14. 7 segment
15. Flip-flop
16. **Let A and B is the input of a subtractor then the borrow will be:**
17. A \* B’
18. A’ \* B
19. A OR B
20. A AND B
21. **The momentary change in the state of flip-flop is called:**
22. Feedback Path
23. Tri State
24. Signals
25. Trigger
26. **Which of the following is the Universal Flip-flop?**
27. S-R flip-flop
28. **J-K flip-flop**
29. Master slave flip-flop
30. D Flip-flop

1. **In digital logic, a counter is a device which:**
2. Counts the number of outputs
3. Stores the number of times a particular event or process has occurred
4. Stores the number of times a clock pulse rises and falls
5. None of the Mentioned

1. **The ROM is a:**
2. Sequential circuit
3. Combinational circuit
4. Magnetic circuit
5. Static circuit

1. **What is the difference between static RAM and dynamic RAM?**
2. Static RAM must be refreshed, dynamic RAM does not.
3. There is no difference.
4. Dynamic RAM must be refreshed, static RAM does not.
5. None of the Mentioned
6. **ASCII stands for:**
7. African Standard Code For Information Interchange
8. American Standard Code For Integer Interchange
9. American Standard Code For Information Interchange
10. African Standard Code For Integer Interchange
11. **There are \_\_\_\_\_\_ cells in a 4-variable K-map.**
12. 4
13. 12
14. 16
15. 18
16. **A variable on its own or in its complemented form is known as a:**
17. Product Term
18. Literal
19. Sum Term
20. None of the Mentioned

1. **The format used to present the logic output for the various combinations of logic inputs to a gate is called a(n):**
2. Boolean constant
3. Boolean variable
4. Truth table
5. Input logic function

1. **The terms "low speed" and "high speed," applied to logic circuits, refer to the \_\_\_\_\_\_.**
2. rise time
3. fall time
4. propagation delay time
5. clock speed

1. **Diagram which is used to show logic elements and their interconnections is said to be:**
2. Circuit diagram
3. System diagram
4. Logic diagram
5. Gate diagram

1. **Electrical circuit having all voltages at one of two values are called:**
2. Binary circuit
3. Binary logic
4. Logic circuit
5. None of the above
6. **System with two states is classified as:**
7. Logic
8. Binary system
9. Binary logic
10. System circuit
11. **Operation carried out by a NOT gate are also termed as:**
12. Inverting
13. Converting
14. Reverting
15. Reversing
16. **Number of logic gates and way of their interconnections can be classified as:**
17. Logical network
18. System network
19. Circuit network
20. Gate network
21. **Logic gate in which output is zero for inputs in which one input is one and other inputs are zero is classified as:**
22. AND gate
23. NOT gate
24. OR gate
25. OUT gate
26. **Logic gate in which any one of inputs is logic 1 results in output as logic 1 is termed as:**
27. NOT gate
28. NOR gate
29. AND gate
30. OR gate
31. **Table that shows result of logical operations conducted is called:**
32. Truth table
33. System table
34. Logic table
35. Circuit table
36. **Logic circuit with only one output and one or more inputs is said to be:**
37. Binary gate
38. Logic gate
39. Circuit gate
40. System gate

1. **A logic gate having two or more inputs and when both inputs are logic 1 then output will be logic 1 is said to be:**
2. OR gate
3. AND gate
4. OUT gate
5. IN gate
6. **The D flip-flop has \_\_\_\_\_\_ input.**
7. 1
8. 2
9. 3
10. 4
11. **Ripple counters are also called:**
12. SSI counters
13. Asynchronous counters
14. Synchronous counters
15. VLSI counters
16. **The first step in the design of memory decoder is:**
17. Selection of a EPROM
18. Selection of a RAM
19. Address assignment
20. Data insertion
21. **NAND function is represented by:**
22. F=x
23. F=(xy)'
24. F=xy
25. F=(x+y)'
26. **The Karnaugh map is also known as:**
27. Veitch diagram
28. Venn diagram
29. Virtual diagram
30. Logic diagram

**SECTION B**

**Short Answer Questions**

**Attempt any five (5) questions out of eight (8) questions (5\*6=30)**

1. Differentiate between combinational logic and sequential logic with examples.
2. Design the 4-bit synchronous up/down counter with timing diagram, logic diagram and truth table. (2+2+2)
3. Given the two binary numbers X = 1010100 and Y = 1000011, perform the subtraction.
4. X -Y (2)
5. Y - X using 2’s complements (2)
6. Express the Boolean function F = xy + x'z in a product of maxterm form (2)
7. Define latches. Explain the programmable logic array. (1+4)

1. Define carry propagation time. Implement Boolean function F (A,B,C) = ∑ (1,3,5,6) with multiplexer. (1+4)
2. Calculate the following:
   * 1. Perform 275+ 484 using BCD.
3. Describe the design procedures for the designing of a combinational circuit.
4. Write short notes on **(any two):** (3+3)
5. SOP & POS
6. Gray code
7. PLA

**SECTION C**

**Long Answer Questions**

**Attempt any two (2) questions out of three (3) questions (2\*20=40)**

1. Draw a block diagram, truth table and logic circuit of 1\*8 Demultiplexer and explain its working principle. (1+2+4+3)
2. Describe the methods of simplifying logic circuits. Simplify the given Boolean function using K map. F(w,x,y,z) = Σ(0,1, 2, 4, 5, 6, 8, 9, 12, 13, 14) (3+7)
3. Explain don’t care conditions. Simplify the Boolean function: (2+8)

(𝑤,𝑥,𝑦,𝑧)= (1,3,7,11,15) that has the don't-care conditions

(𝑤,𝑥,𝑦,𝑧) = (0,2,5)

1. Describe JK master slave flip-flop. Design its logic circuit, truth table and explain the working principle. (2+ 2+3+3)

1. State De Morgan’s theorem. Reduce the given Boolean expression to minimum number of literals: (4+6)

AB + (AC)’ + AB’C(AB + C)

1. Explain code conversion. Design a BCD to Excess 3 code converter circuit with truth table, Boolean expression and logic circuit. (2+8)

**\*\*\*BEST OF LUCK\*\***